CSE 417 Final Project

Submission deadline: 18 January 2017, @9am.

Presentations: 18 - 19 January 2017. You must present your project, otherwise you will get zero.

In this project, you will write a Verilog code to perform the following actions:

1. The main loop consists of a timer. The program is as follows:

```
timer = 0;
while(1) {
   for i=1:A
        for j=1:B
            //do nothing
        next j
   next i
   timer++
   print timer to the first two 7-segment display
}
```

You need to adjust the number of nested loops (ie 2, 3, 4, 5, ? loops) and ranges (A, B, C, etc) to make sure that a delay of 1 sec is achieved. The timer increments at approximately every second. The value of timer is displayed at the first two 7-segment display.

2. Two pushbuttons are connected to programmable interrupt controller (PIC) and trigger ISR. In other words, when any of pushbuttons are pressed, the CPU stops what it is doing and jumps to the corresponding ISR. When the ISR is finished, it returns the main code (timer) and resumes running.

3. The corresponding ISR will be executed, when a pushbutton is pressed.
    a. When pushbutton 1 is pressed, the value in the last two seven segment registers will be INCREMENTED by 2 (must never increment beyond 0xFF) and displayed at last two seven segment displays.

    b. When pushbutton 2 is pressed, the value in the last two seven segment registers will be DECREMENTED by 1 (must never decrement below 0) and displayed at last two seven segment displays.

4. You must implement PIC in Verilog.

Note: You do not need to make any hardware changes, you must only write the Verilog code.