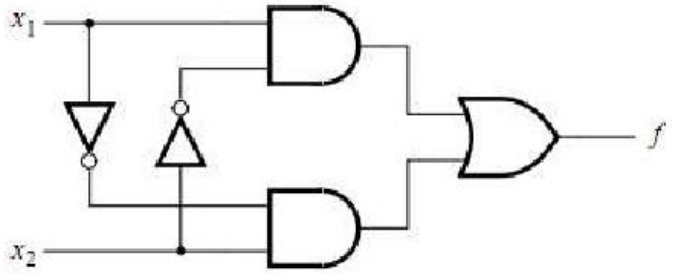
USING QUARTUS II SOFTWARE

Each logic circuit, or subcircuit, being designed with Quartus II software is called a project. The software works on one project at a time and keeps all information for that project in a single directory (folder) in the file system.

The running example for this lab experiment is a simple circuit for two-way light control circuit shown in Figure 1. The procedure is exhibited step by step in the lab.



x_1	x_2	f
0	0	0
0	1	1
1	0	1
1	1	0

Figure 1. The two-way light control circuit

- Note that this is just the Exclusive-OR function of the inputs x1 and x2, but we will specify it using the gates shown in the figure.

Starting a New Project:

- Start the Quartus II software. You should see a display similar to the one in the Figure 2.

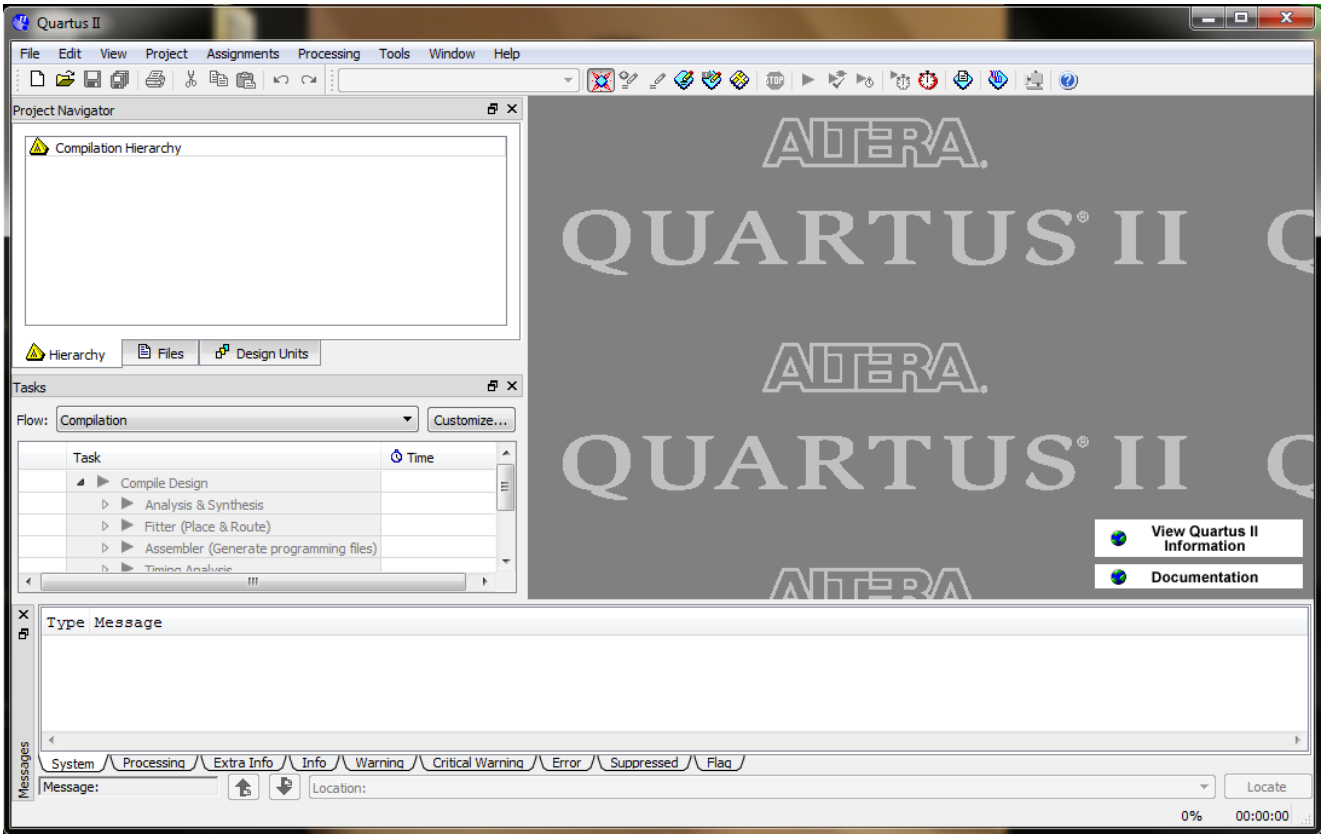


Figure 2. The main Quartus II display

- Select **File > New Project Wizard** to reach the window in Figure 3

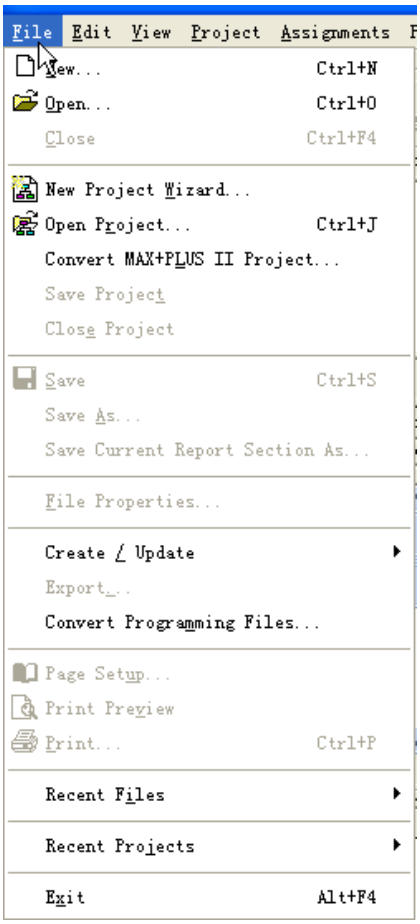


Figure 3. File menu

- Check the box **Don'tshow me this introduction again** in the Figure 4 Press **Next** to get the window shown in Figure 5.

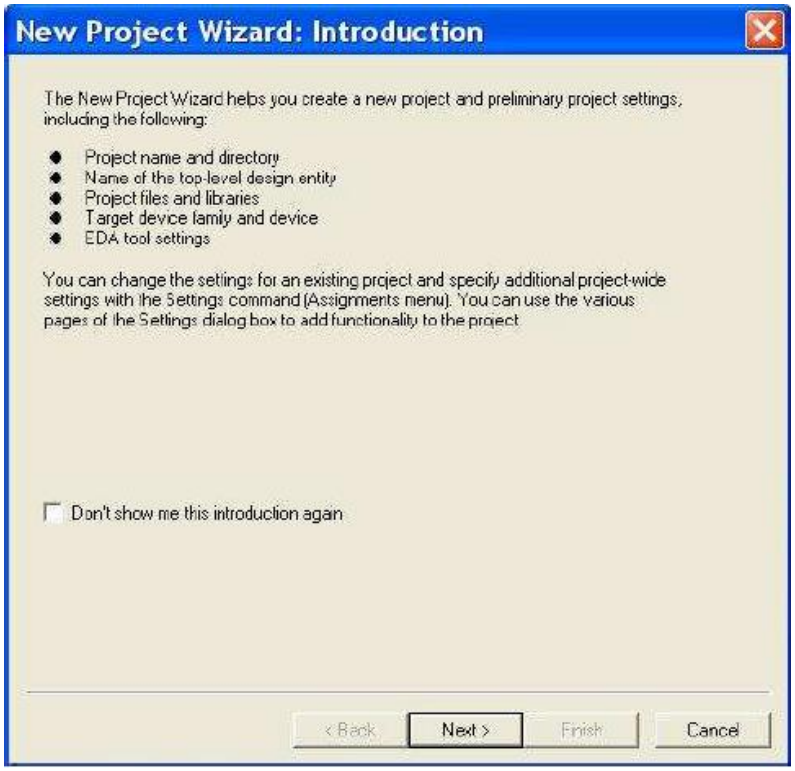


Figure 4. Tasks performed by the wizard

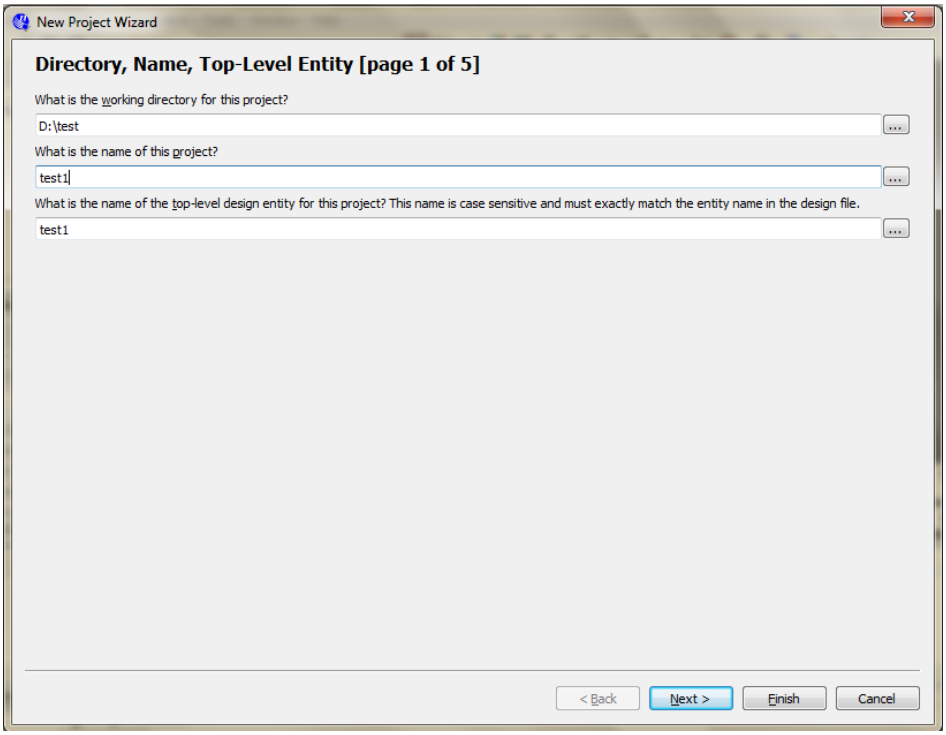


Figure 5. Cration of a new project

- Press **Next**, then you should see attention of the Figure 6.

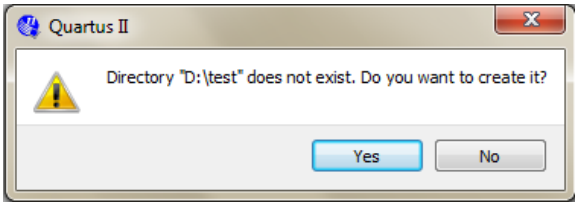


Figure 6. Create a new directory for the project

- Click **Yes**, which leads to the window in Figure 7.

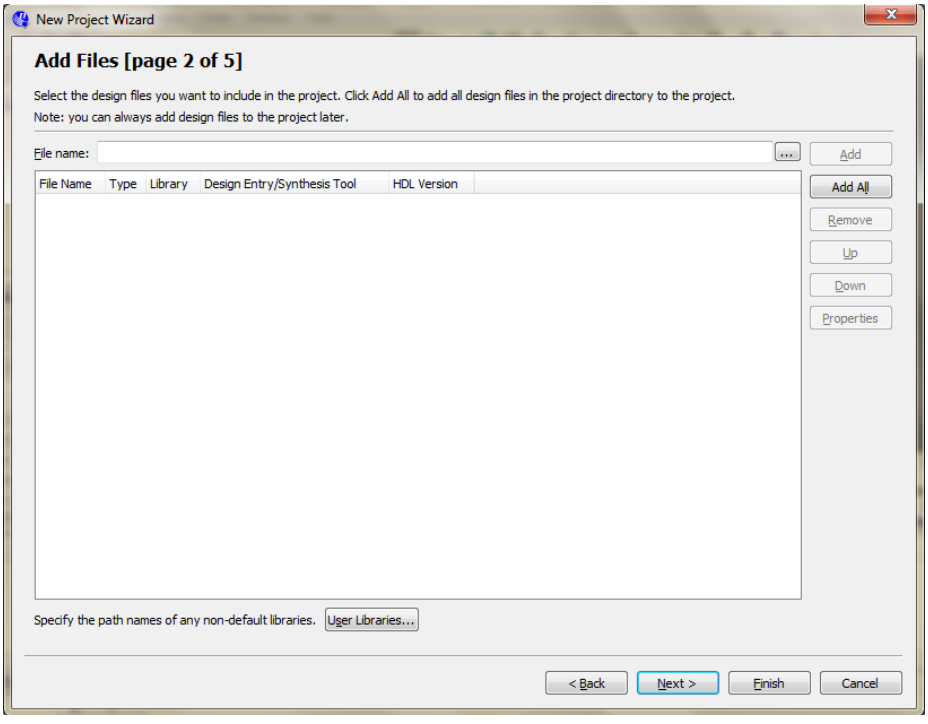


Figure 7. The wizard can include user-specified design files.

- The wizard makes it easy to specify which existing files (if any) should be included in the project. Assuming that we do not have any existing files, Click **Yes**, which leads to the window in Figure 8.

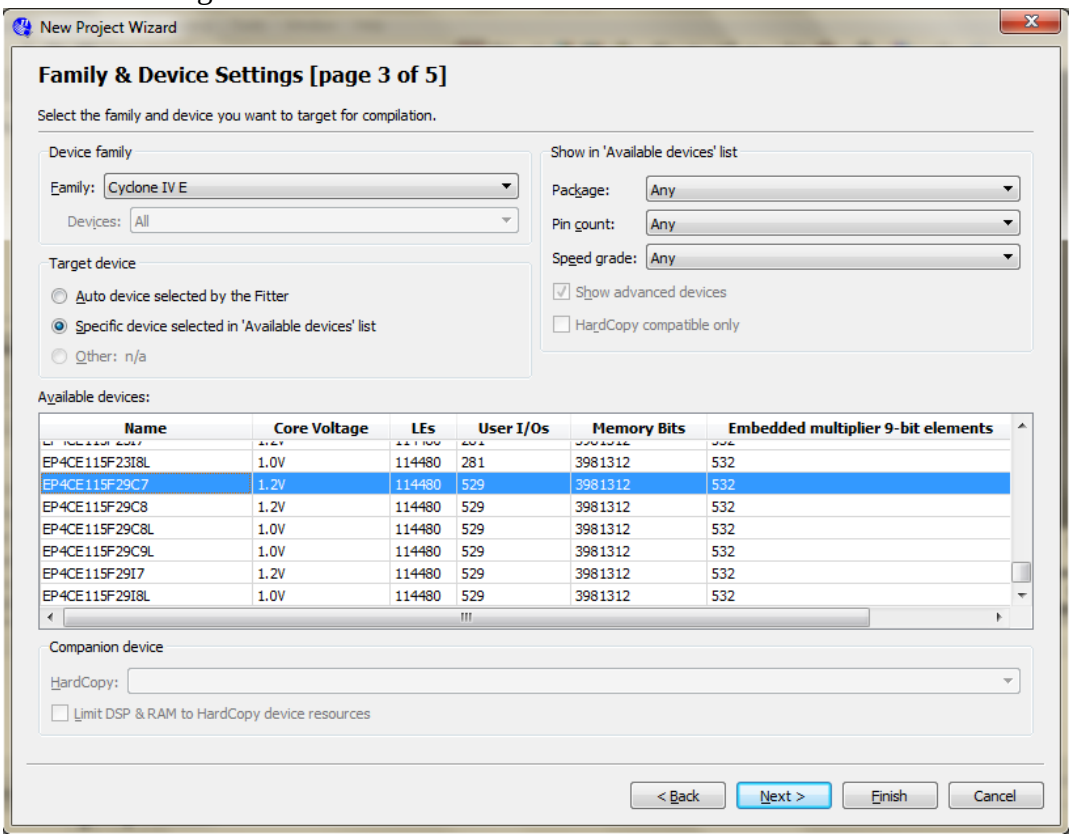


Figure 8. Choose the FPGA metarial.

- We have to specify the type of device in which the designed circuit will be implemented. Choose Cyclone IV E as the target device family and the device called EP4CE115F29C7 which is the FPGA used on Altera's DE2-115 board. After doin theese steps click **Next,** which open window in Figure 9.

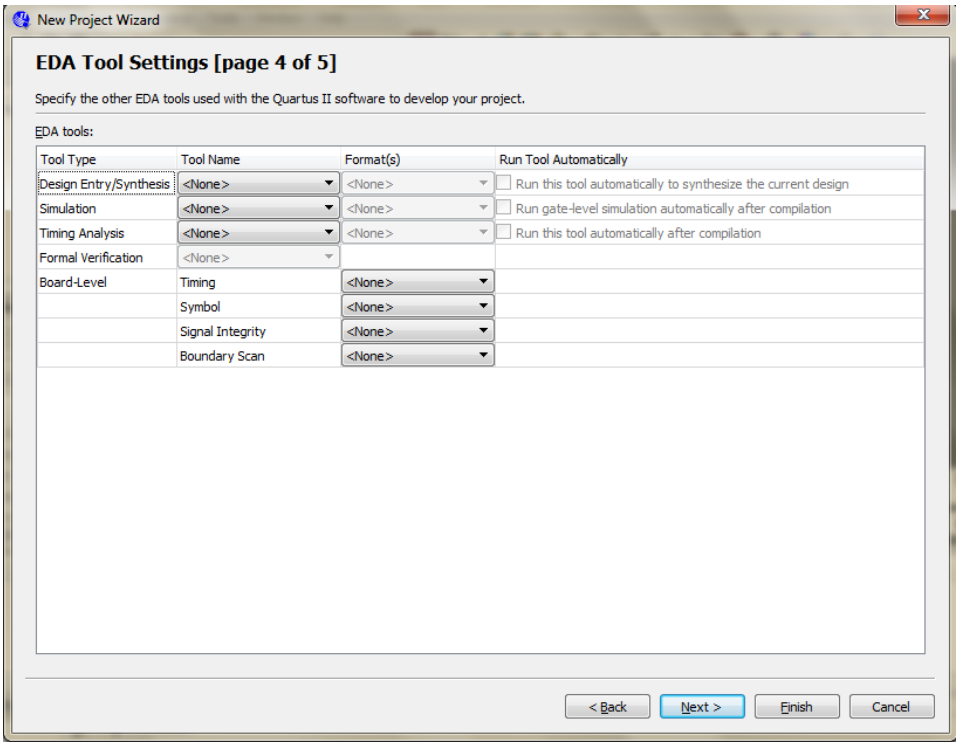


Figure 9. Other EDA tools can be specified.

- EDA acronym stands for Electronic Design Automation (refer to third-party tools). Choose **None** for all options and press **Next,**

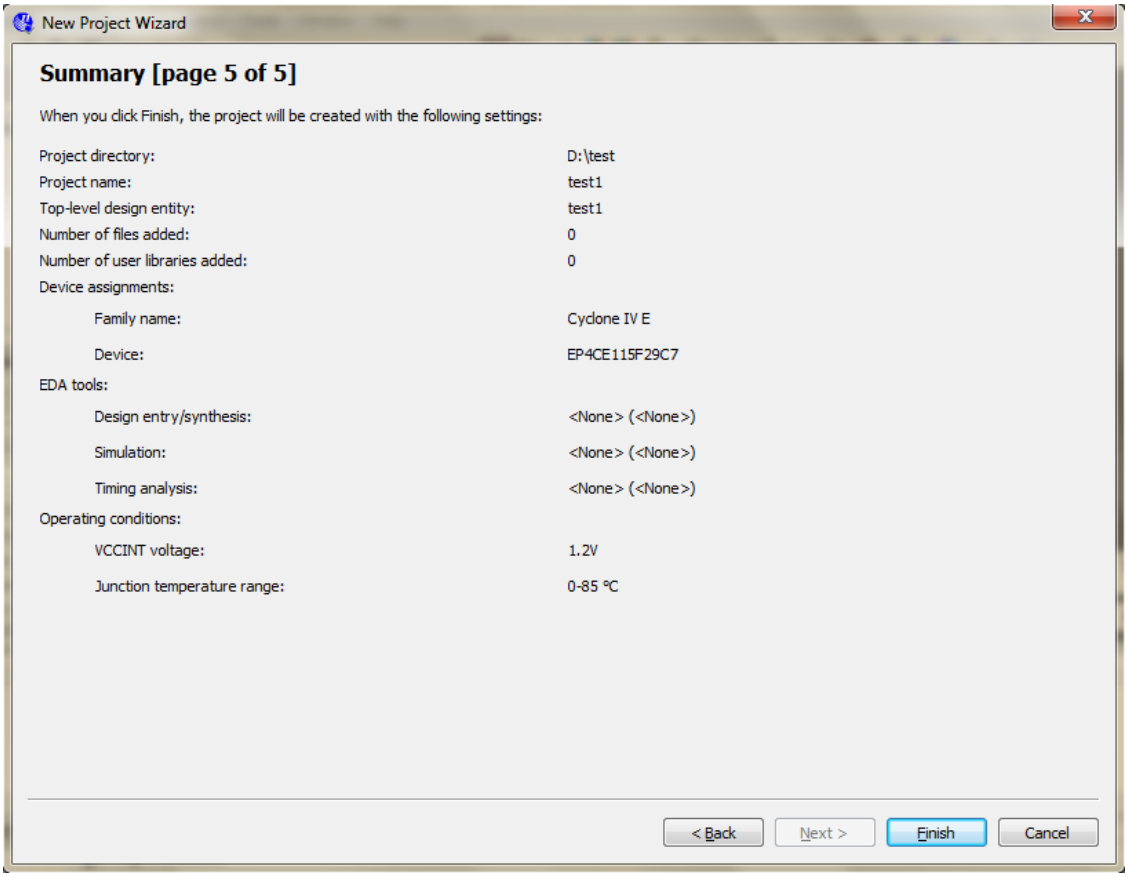


Figure 10. Summary of the project settings.

- Press **Finish,** The window in the Figure 11 is showed.

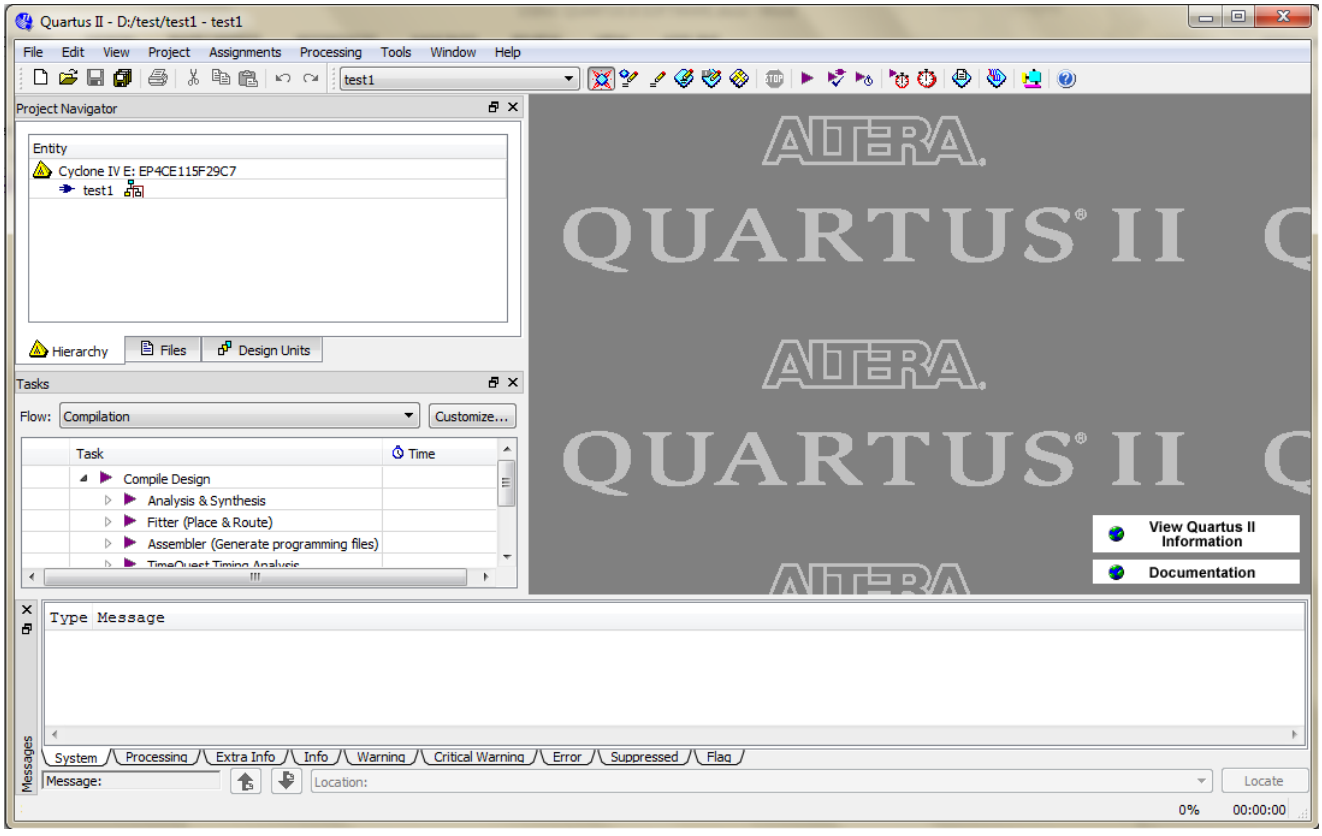


Figure 11. The Quartus II display for the created project.

Design Entry Using Verilog Code:

- Select **File > New** to get the window in Figure 14. Choose **Verilog HDL File** and click **OK.**

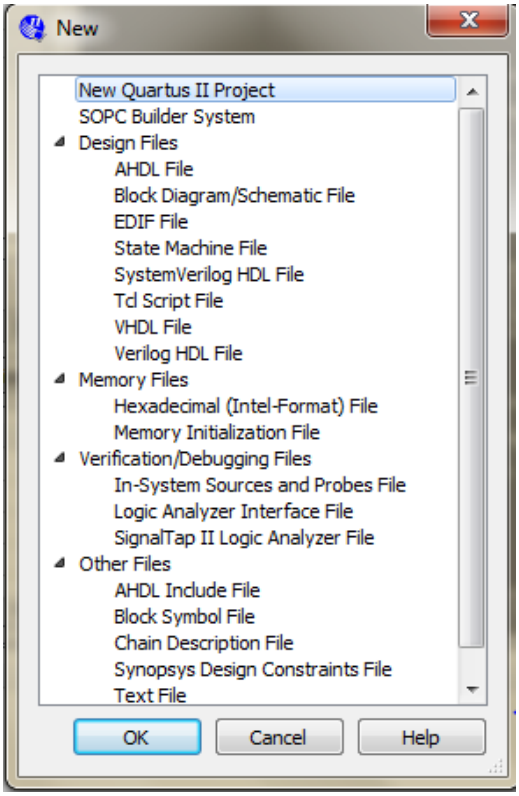


Figure 14. Choosing the new file type.

- This open the text editor window. Select File > Save As to open the pop-box depicticated in Figure 15.

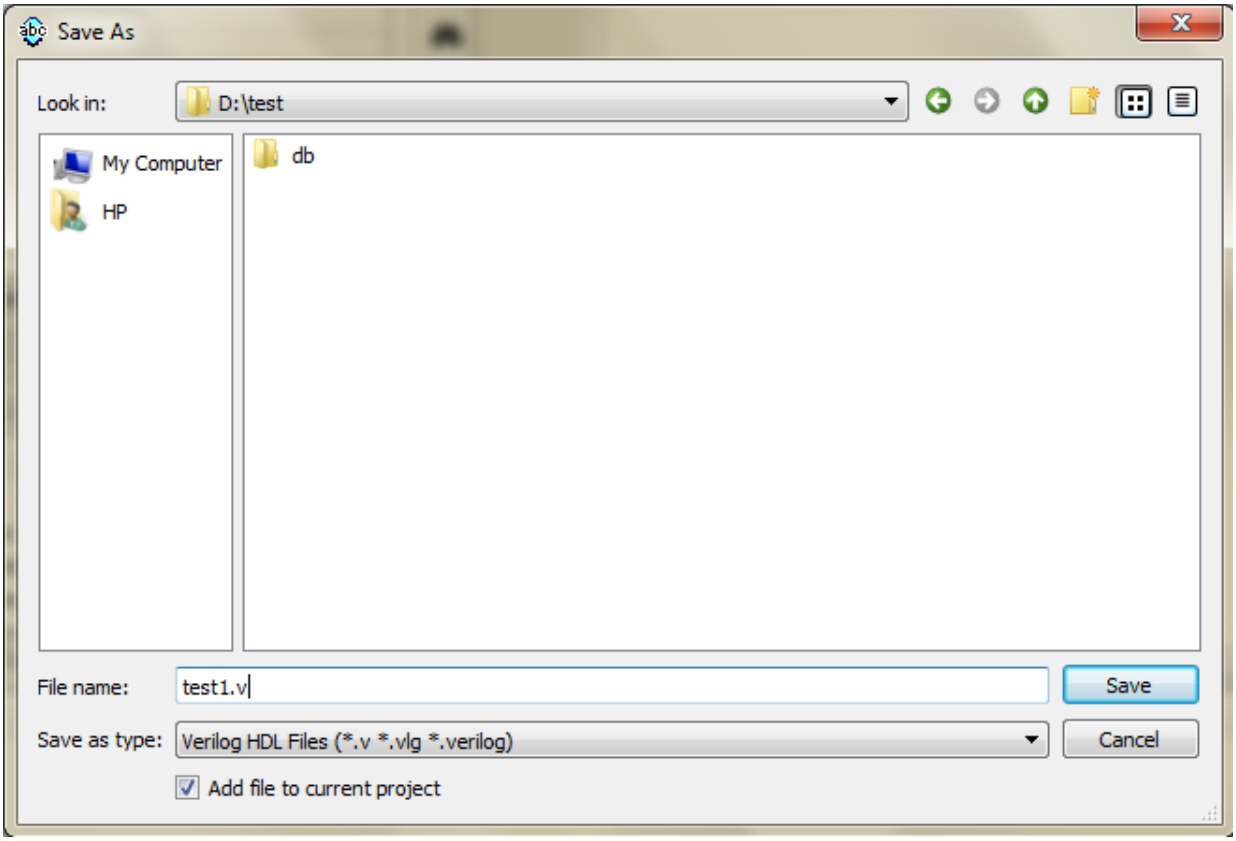


Figure 15. Name the file

- Write the same name Verilog HDL File and checkmark in the box. Click **Save,**

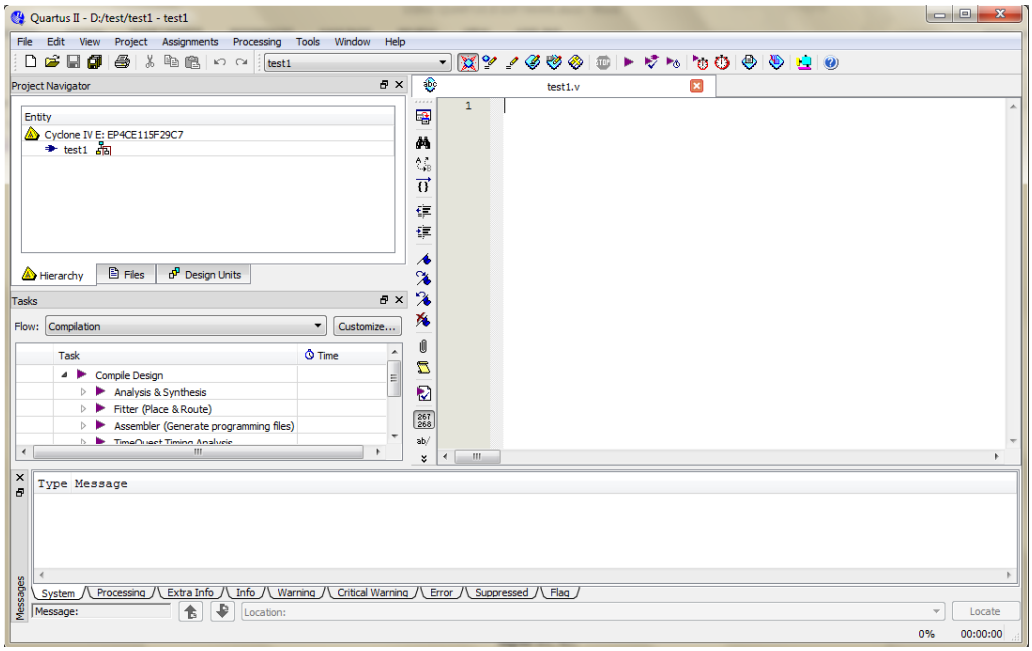


Figure 16. Text Editor

- Write verilog code which belongs to the two-way light control circuit in Figure 16;

```
module test1 (x1, x2, f);
    input x1, x2;
    output f;
    assign f = (x1&~x2) | (~x1&x2);
endmodule
```

or;

```
module test1 (x1, x2, f);
    input x1, x2;
    output f;
    wire w1, w2;
    not notS0(nx1, x1);
    not notS1(nx2, x2);
    and A1(w1, x1,nx2);
    and B1(w2, nx1,x2);
    or(f, w1, w2);
endmodule
```

- **Click Assignments > Settings**, which leads to the window in Figure 17

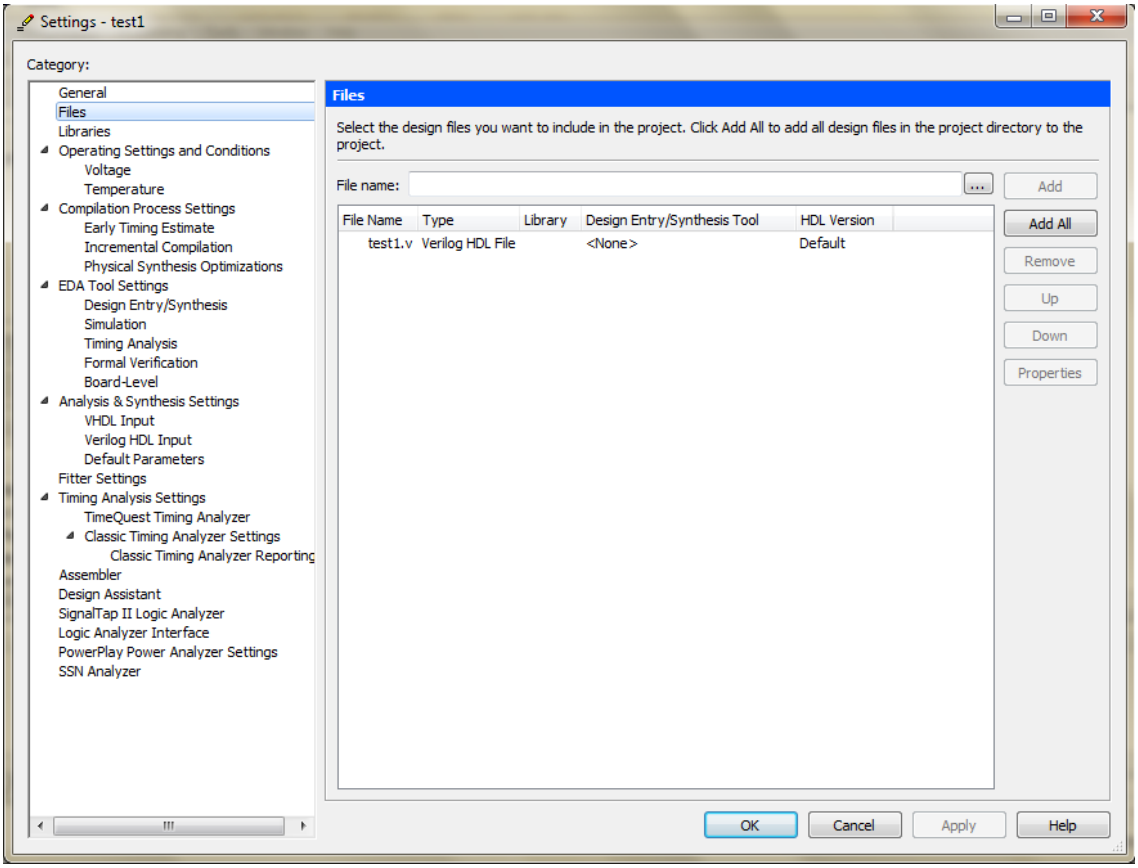


Figure 17. Settings window

- Test1.v must be added in the window. If it isn't, you add the **add/remove** part. Click **OK**

Compiling:

- Click **Processing > Start Compilation**,

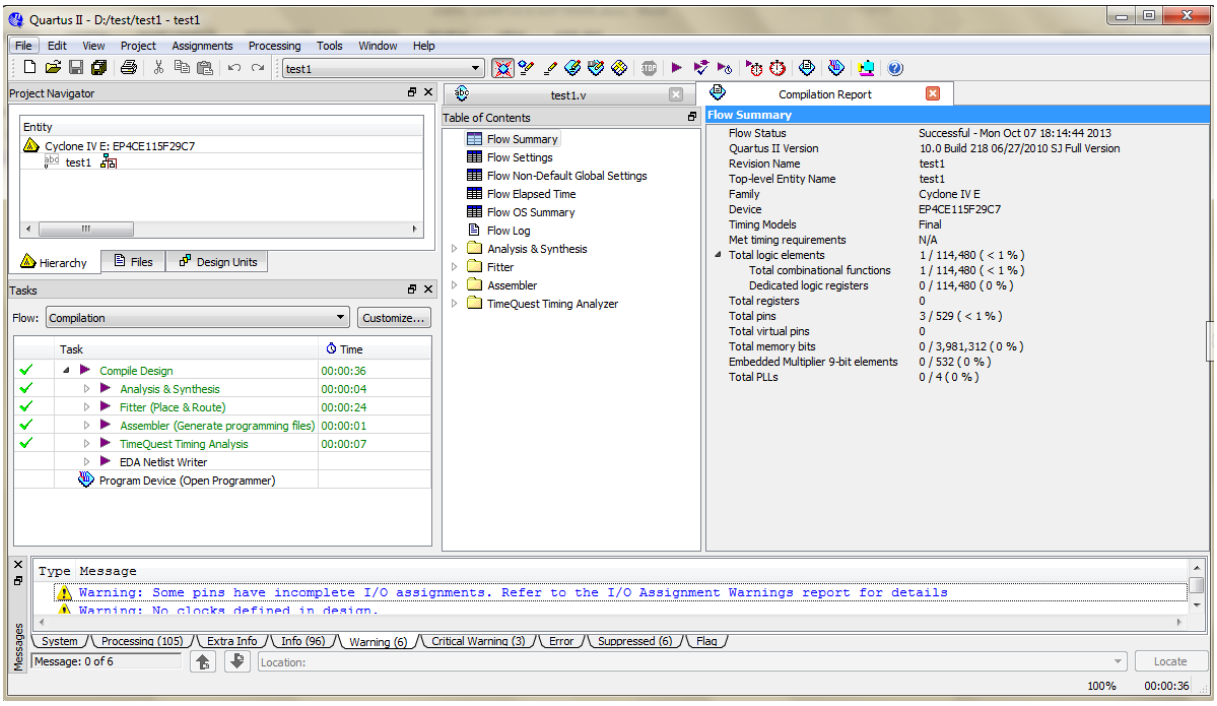


Figure 18. The Compilation report and message part.

Pin Assignments:

- Click **Processing > Pin Planner,**

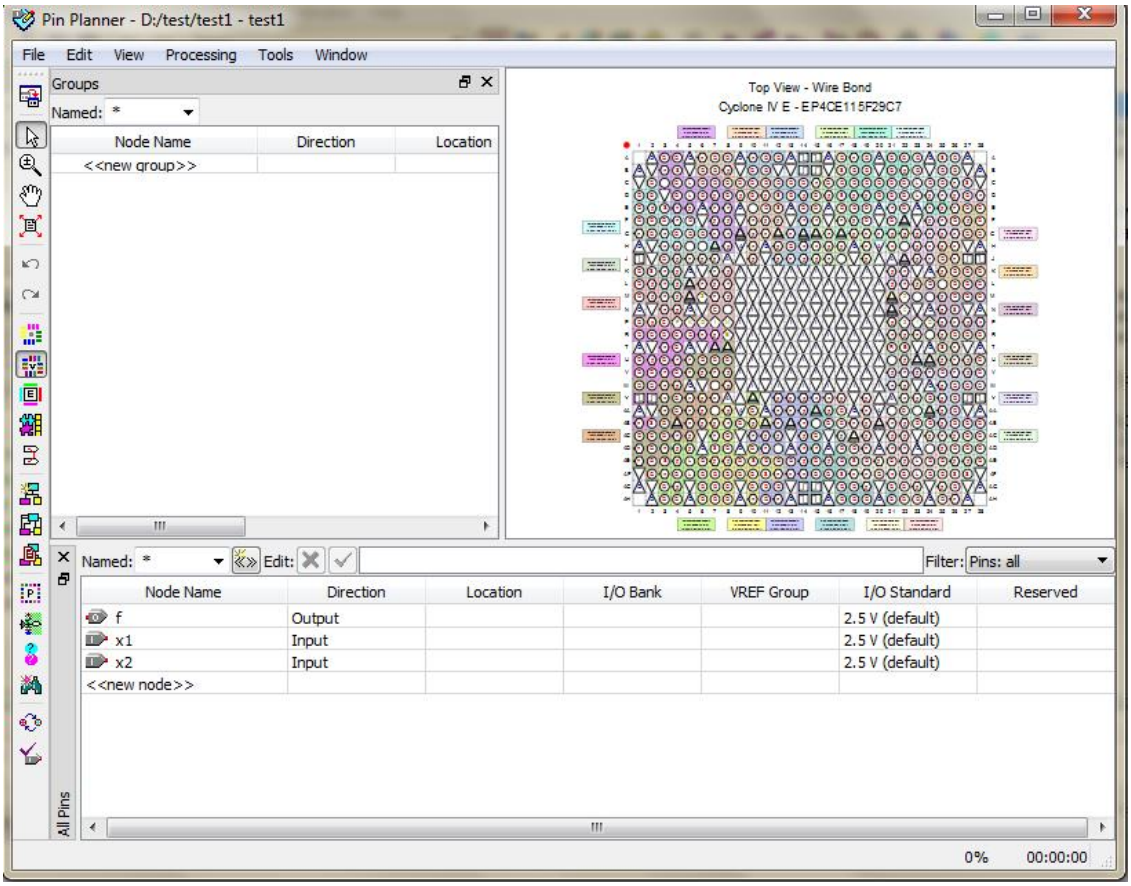


Figure 19. Pin settings

- Click twice the location and set the SW0, SW1, LED0 pins,

SW0	AB28
SW1	AC28
LED0	E21

The **File > Save** is pressed.

- Again Click **Processing > Start Compilation**

Programming and Configurating the FPGA Device:

- ***JTAG Programming:***

The FPGA device must be programmed and configured to implement the designed circuit. The required configuration file is generated by the Quartus II Compiler's Assembler module. Altera's DE2-115 board allows the configuration to be done in two different ways, known as JTAG and AS modes. The configuration data is transferred from the host computer (which runs the Quartus II software) to the board by means of a cable that connects a USB port on the host computer to the leftmost USB connector on the board. To use this connection, it is necessary to have the USB-Blaster driver installed. If this driver is not already installed, consult the tutorial Getting Started with Altera's DE2-115 Board for information about installing the driver. Before using the board, make sure that the USB cable is properly connected and turn on the power supply switch on the board.

In the JTAG mode, the configuration data is loaded directly into the FPGA device. The acronym JTAG stands for Joint Test Action Group. This group defined a simple way for testing digital circuits and loading data into them, which became an IEEE standard. If the FPGA is configured in this manner, it will retain its configuration as long as the power remains turned on. The configuration information is lost when the power is turned off. The second possibility is to use the Active Serial (AS) mode. In this case, a configuration device that includes some flash memory is used to store the configuration data.

Quartus II software places the configuration data into the configuration device on the DE2-115 board. Then, this data is loaded into the FPGA upon power-up or reconfiguration. Thus, the FPGA need not be configured by the Quartus II software if the power is turned off and on.

The choice between the two modes is made by the **RUN/PROG** switch on the DE2-115 board. The **RUN** position selects the JTAG mode, while the **PROG** position selects the AS mode.

- Connect the FPGA device to computer and power on. Flip the **RUN/PROG** switch into the **RUN** position. **Select Tools > Programmer** in the Figure 18, the open window is Figure 20

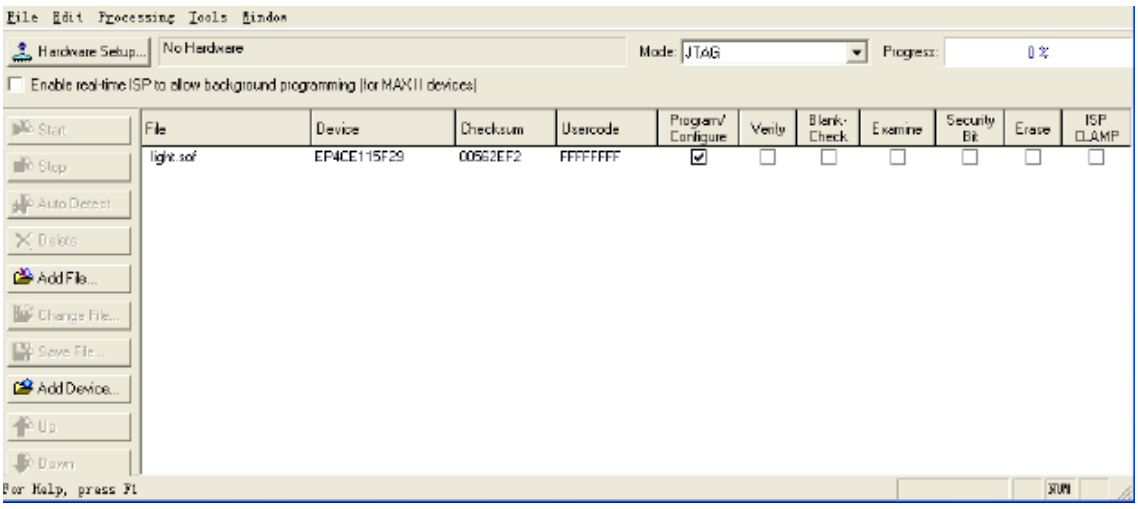


Figure 20. Programmer

- Press the **Hardware Setup** and choose **USB-Blaster,** and choose **JTAG** model. Test1.sof must be seen in the window. Choose the file and press **Start.** Check the truth table using SW0, SW1 and LED0 at the FPGA Device.

The other way of the programming is shown later.