Due Date: 29.10.2018

EE 311 LT-SPICE HW#1

Q-1) Consider the following circuit as illustrated in Fig.1. Apply a sinusoidal voltage supply to the input with $20V_{p-p}$ and 50Hz. Select time domain analysis for 100ms.

a) Construct this circuit in LT-SPICE for "Ideal Diode" model with zero on resistance. Plot input voltage, diode current and output voltages.

b) For ideal diode model in a), calculate ripple voltage value (V_r) and maximum diode current (i_{Dmax}).

c) Construct this circuit with "diode.txt" of CMOS Spice Lib Files at the website.

d) Repeat calculations in b) for construction in step of c) with "diode txt" model.

e) Compare results of ideal model and "diode.txt" and explain differences.

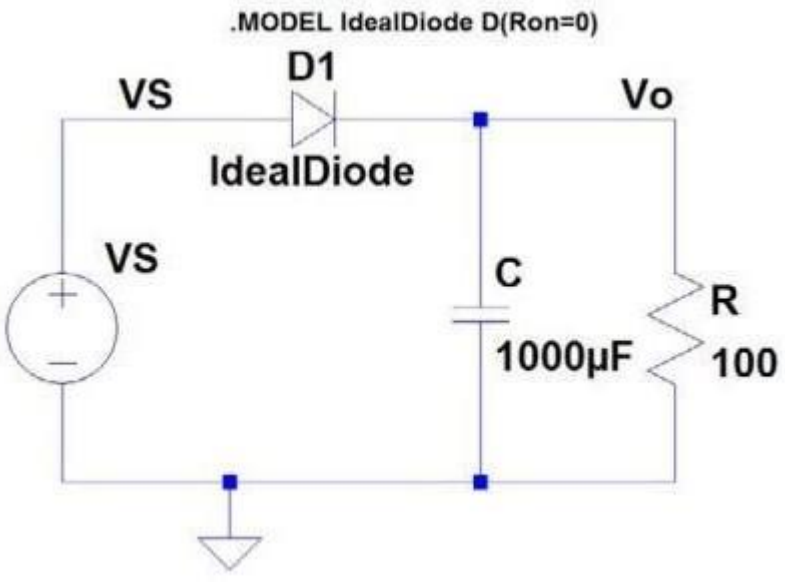

Fig.1: Half Wave Rectifier With a Smoothing Filter

Q-2) Consider the Fig.2.

a) In this circuit, calculate τ comes from capacitor and resistors.

b) Calculate capacitor voltage at the time of τ.

c) Construct the circuit in LT-SPICE with PWL source for transient simulation of 8ms as depiced in Fig.2. In here, PWL source should start with zero value. After that, it has a pretty good rising time as a 2us and it goes up to the 6V. It stays at 6V for a 3ms. Then it decreases all of a sudden with falling time of 0.2us. It is ended up with zero volt. In this respect, check the capacitor voltage that you calculated in b). **Hint:** Utilize from cursor attachment. Show the results. Comment on the differences between your calculation and SPICE's result.

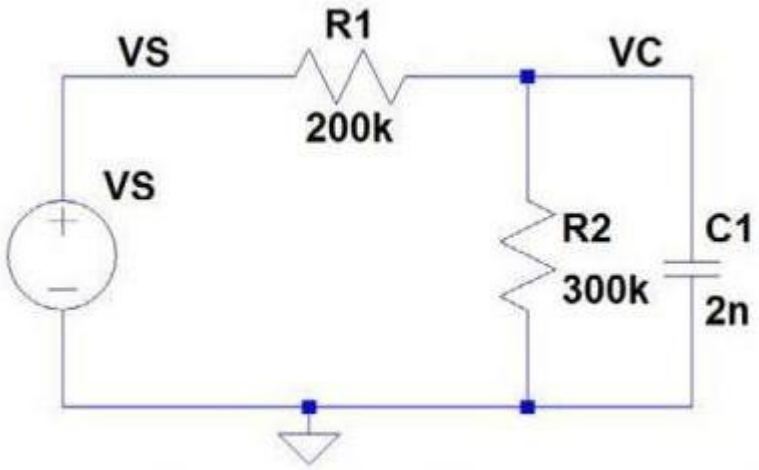

Fig.2: A RC network with PWL source

NOTE: Please, show all your calculations step by step for partially credit.