EXPERIMENT 1

FAMILIARIZATION WITH DIGITAL PULSE AND MEASUREMENTS OF THE TRANSIENT TIMES

REFERENCES

Analysis and Design of Digital Integrated Circuits, Hodges and Jackson, pages 6-7
Experiments in Microprocessors and Digital Systems, Douglas V.Hall, pages 1-4

OBJECTIVES

At the conclusion of this laboratory exercise, you should be able to:

1. Set the controls of the oscilloscope and signal generator to obtain a visible, clear, stable, and calibrated trace of a digital pulse.
2. To measure transient characteristics of a digital pulse.

EQUIPMENT

1 Triggered sweep laboratory oscilloscope (dual trace preferred)
1 Probe for oscilloscope
1 Laboratory function generator

MATERIALS

None

DISCUSSION

Specific definitions of pulse transition times and propagation delay times are needed for a description of the dynamic characteristics of logic circuits. Once such definitions are established, calculations of these times can be made. Standart definitions of digital circuit delay times are illustrated in Figure 1. Rise and fall times t_f and t_r are defined between the 10 and 90% points of the total transition at the input of an inverter circuit or gate. Pulse width PW of the pulse is the time between 50% points of the rising and falling edge of the pulse. Cycle time t_{cyc} is the time between the 50% points of successive cycles in the signal waveform.

PROCEDURE

1. Set the function generator for a square wave of 1kHz.
2. Set the oscilloscope for 1V/div.
3. Adjust the amplitude control of the generator to produce a 5V peak to peak square wave as measured on the oscilloscope.
4. Switch the oscilloscope to GND, and use the vertical position control to set the trace on the bottom horizontal graticule line of the screen. (leave this control set at this position: this estabishes the bottom graticule line as 0V dc reference.)
5. Switch the oscilloscope to dc coupling .

6. Now turn on the offset control on the function generator, and adjust it until the bottom line of the square wave rests on the bottom graticule. The top of the waveform should be five divisions above the bottom graticule line (Note: if you switch the coupling to grorund, the horizontal trace should still be resting on the bottom graticule line as 0V reference.)
7. If your generator has variable symetry capability, select this function and adjust the variable symetry control to obtain a 1kHz pulse with a 20 percent duty cycle. (The percentage of cycle equals the time that the pulse is high W divide by the total time of a complete cycle T, times 100, or W/T x 100.)

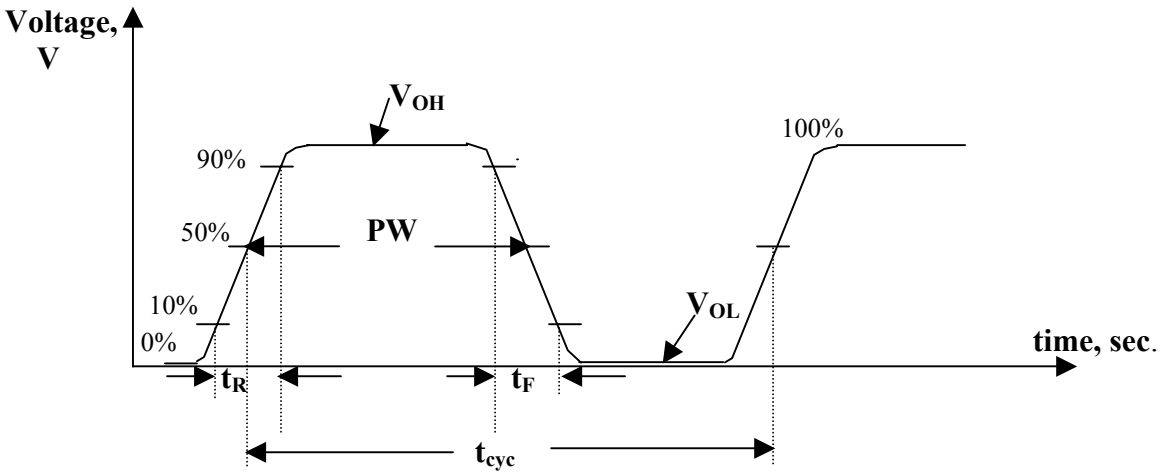


Figure 1.1 Definition of transient and delay times of a digital pulse

8. Carefully observe Figure 1.1 and measure and record t_R, t_F, PW, and t_{CYC} of digital pulse and sketch the waveform. (NOTE: use horizontal magnification in order to measure t_D, t_R, t_F more accurate.)

9. Repeat the procedure 8, for 10kHz, 100kHz and 1MHz.

EXPERIMENT 2

TRANSISTOR INVERTER

REFERENCES

Analysis and Design of Digital Integrated Circuits, Hodges and Jackson, pages 187-232.

OBJECTIVES

At the conclusion of this laboratory, you should be able to:

1. Build a basic inverter circuit.
2. Measure various voltages of inverter circuit.
3. Plot a static transfer curve for a inverter.
4. Use a transfer curve to determine V_{IL}, V_{IH}, V_{OH}, V_{OL}, N_{ML}, and N_{MH} .
5. Calculate fan-out of the inverter from the experimental results.
6. Measure various voltages and delay times of inverter circuit under a simulated maximum load.

EQUIPMENT

Osilloscope, signal generator, dc voltmeter, dc milliammeter and 5V power supply.

MATERIALS

2 2N 2222 transistor, 1 10k resistor, 2 1k resistor

PROCEDURE

1. Connect the circuit shown Figure 2.1 but with no load at V_{O1}. Start with V_{I1}=0V, and measure V_{O1} at each 0.05 V increments of V_{I1} and record them in Table 2.1.

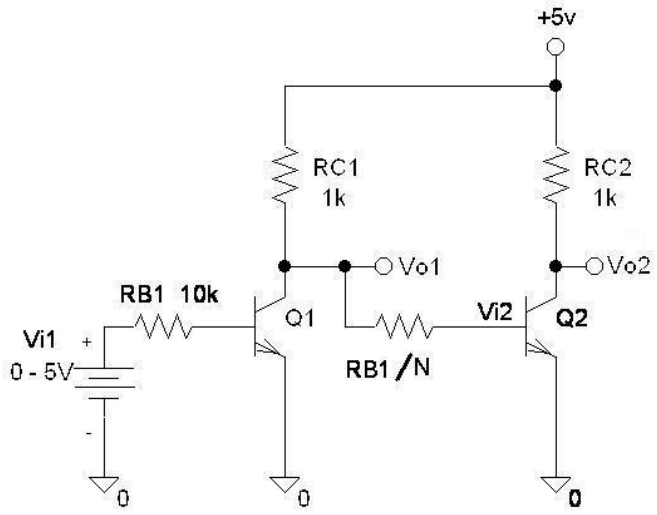
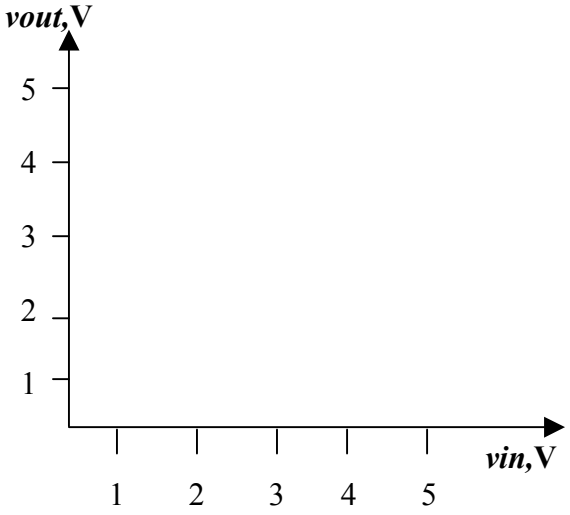


Figure 2.1 Transistor inverter

V_{I1} (volts)	V_{O1}(volts)	V_{I1} (volts)	V_{O1}(volts)	V_{I1} (volts)	V_{O1}(volts)
0		0.75		1.5	
0.05		0.8		1.55	
0.1		0.85		1.6	
0.15		0.9		1.65	
0.2		0.95		1.7	
0.25		1		1.75	
0.3		1.05		1.8	
0.35		1.1		1.85	
0.4		1.15		1.9	
0.45		1.2		1.95	
0.5		1.25		2.0	
0.55		1.3		2.05	
0.6		1.35		2.1	
0.65		1.4		2.15	
0.7		1.45		2.2	

Table 2.1 V_{O1} versus V_{I1}

2. Plot V_{O1} versus V_{I1}, and determine V_{OH}, V_{OL}, V_{IL}, N_{MH} and N_{ML} and calculate fan-out of the circuit.



V_{IL} =_ V_{IH} = V_{OH} = _ V_{OL} =

N_{MH} = V_{OH} -V_{IH} = N_{ML} = V_{IL} - V_{OL} =

Fan-out	$N \leq \beta_F \dfrac{V_{CC}-V_{BE(sat)}}{V_{CC}-V_{CE(sat)}} - \dfrac{R_B}{R_C} =$

3. Connect the circuit as shown Figure 2.1 and measure voltages V_{I1}, $V_{O1,}$ $V_{I2,}$ V_{O2} and times as indicated in Figure 2.2 and sketch the output waveforms.

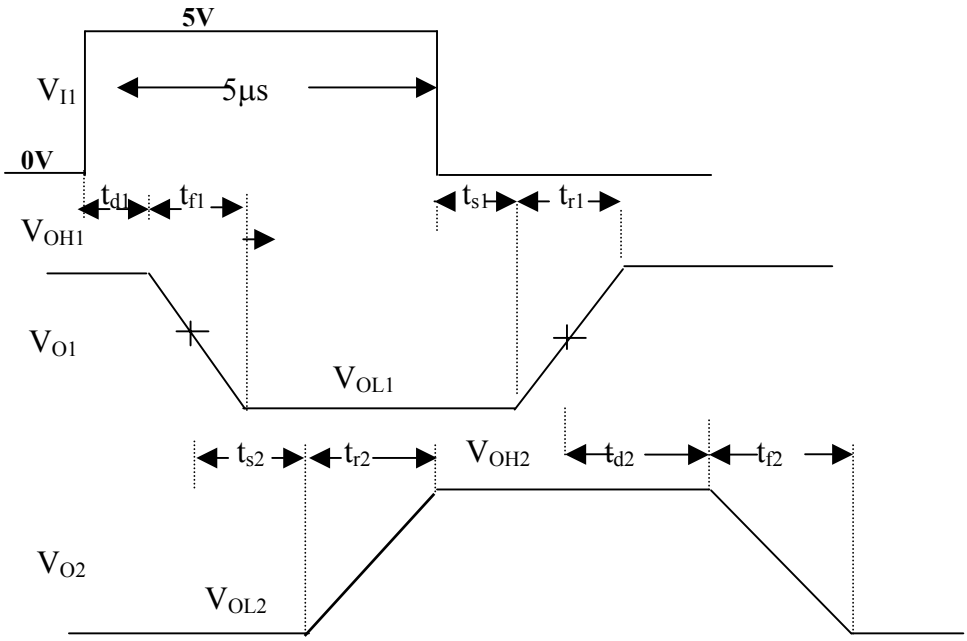


Figure 2.2 Definition of transient and delay times

EXPERIMENT 3

LOGIC GATES AND TTL 74LS SERIES CHARACTERISTICS

REFERENCES

Analysis and Design of Digital Integrated Circuits, Hodges and Jackson, pages 241-246
Experiments in Microprocessors and Digital Systems, Douglas V.Hall, pages 5-9

OBJECTIVES

At the conclusion of this laboratory, you should be able to:

1. Use a data sheet to determine the fan-out, noise margin and output current specifications for a TTL LS gate.
2. Measure typical output voltage levels and input current requirements for a TTL LS gate.
3. Measure the typical output low voltage level under a simulated load condition.
4. Plot a static transfer curve for a TTL LS NAND gate.
5. Use the x-y mode of an oscilloscope to obtain a dynamic transfer curve for a TTL LS inverter.
6. Use a transfer curve to obtain useful data regarding the threshold voltage, $\mathbf{V_{IHmin}}$, $\mathbf{V_{ILmax}}$, and noise margins for a TTL LS gate .

EQUIPMENT

Osilloscope, signal generator, dc voltmeter, dc milliammeter and 5V power supply.

MATERIALS

1 74LS00 TTL IC NAND gate, 2 Si diode, 1 100 Ω and 1 1kΩ resistor,

PROCEDURE

1. Read the TTL data sheet pages for a quad 74LS00 two input NAND gate. Find and record the following information:

   - ☑ The logic diagram of the device, with pin numbers.
   - ☑ The recommended operating supply voltage $V_{CC.}$
   - ☑ The minimum input high voltage V_{IH} and the maximum input low voltage V_{IL}.
   - ☑ The typical output high voltage V_{OH} and the typical output low voltage V_{OL}.
   - ☑ The input high and input low currents I_{IH} and I_{IL}, respectively.
   - ☑ The maximum output high output high current I_{OH} and the output low current I_{OL}.

2. Connect the circuit shown Figure 3.1. Apply 100 Hz 5V peak sinusodial signal to the input. Calibrate the oscilloscope for equal vertical and horizontal scales.
3. Carefully sketch the VTC of the circuit, labeling all asymptotic voltages and breakpoints. Do this for:
   (a) A fan-out 1, as in Figure 3.1(a)
   (b) A fan-out of 10, as in Figure 3.1(b)

4. What are the noise margins N_{MH} and N_{ML} for the two cases of fan-out?

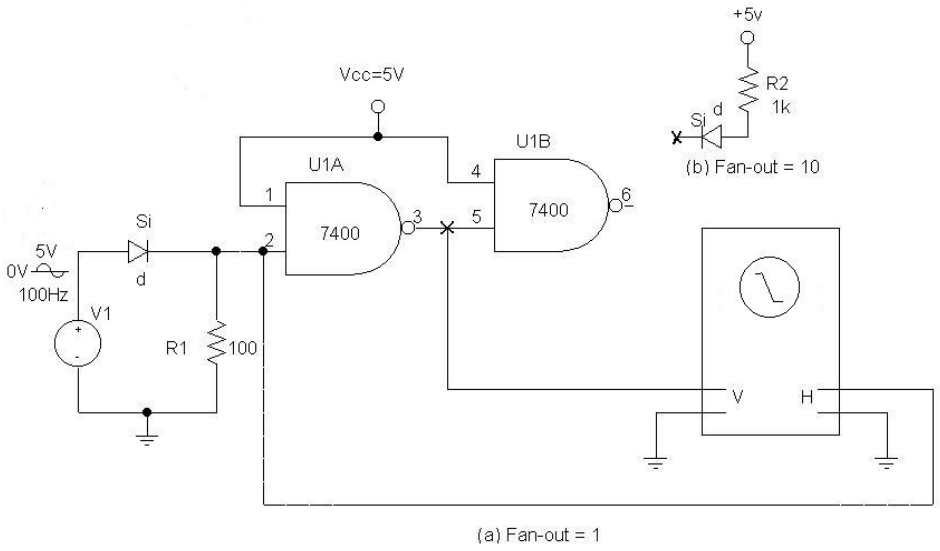


Figure 3.1

5. Measure and record I_{in} while V_{in} is varied from -0.5V to +5V and plot I_{in} versus V_{in}.

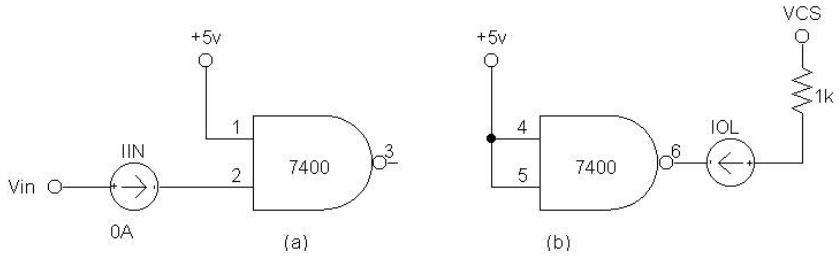


Figure 3.2

6. Measure and record I_{OL} while V_{CS} is varied from –5V to +15V and plot I_{OL} versus V_{CS}.
7. Comment on the reason for the slope of these curves, especially as the input and output voltages go negative.

EXPERIMENT 4

CMOS 74HC SERIES CHARACTERISTICS

REFERENCES

Analysis and Design of Digital Integrated Circuits, Hodges and Jackson, pages 57-103.
Experiments in Microprocessors and Digital Systems, Douglas V.Hall, pages 13-15

OBJECTIVES

At the conclusion of this laboratory, you should be able to:

1. Use a data sheet to determine the fan-out, noise margin and output current specifications for a CMOS gate.
2. Measure the typical output low voltage level under a simulated load condition.
3. Plot a static transfer curve for a CMOS NAND gate.
4. Use the x-y mode of an oscilloscope to obtain a dynamic transfer curve for a CMOS inverter.
5. Determine the relationship between power dissipation and frequency.
6. Determine unwanted voltages on V_{DD} at upper frequencies and under load.

EQUIPMENT

Osilloscope, signal generator, dc voltmeter, dc milliammeter and 5V power supply.

MATERIALS

1 74HC00 CMOS IC NAND gate, 1 Si diode, 1 100 Ω resistor, 1 47pF and 1 100nF capacitor.

PROCEDURE

1. MOS and CMOS component handling precautions must be considered before you begin to work with. Therefore you are expected to read from text books about precautions of handling CMOS. Some are precautions are emphasized here.

   - ☑ When working with MOS and CMOS always apply dc supply power to the circuit before applying the signal to the input.
   - ☑ Always remove the signal source from the gate input before turning off the dc suppy voltage.
   - ☑ For MOS families, inputs should never be left open.
   - ☑ Always set input signals so they do not exceed the minimum V_{IH}. For the CMOS device in this experiment, $V_{IL}=V_{SS}$ (or ground) and $V_{IH} = V_{DD}$ (which is 5V for this experiment)

2. Read the CMOS data sheet pages for a quad 74HC00 two input NAND gate. Find and record the following information:

   - ☑ The logic diagram of the device, with pin numbers.
   - ☑ The recommended operating supply voltage $V_{CC.}$

- ☑ The minimum input high voltage V_{IH} and the maximum input low voltage V_{IL}.
- ☑ The typical output high voltage V_{OH} and the typical output low voltage V_{OL}.
- ☑ The input high and input low currents I_{IH} and I_{IL}, respectively.The maximum output high output high current I_{OH} and the output low current I_{OL}.

2. Connect the circuit shown Figure 4.1. Apply 100 Hz 5V peak sinusodial signal to the input. Calibrate the oscilloscope for equal vertical and horizontal scales.

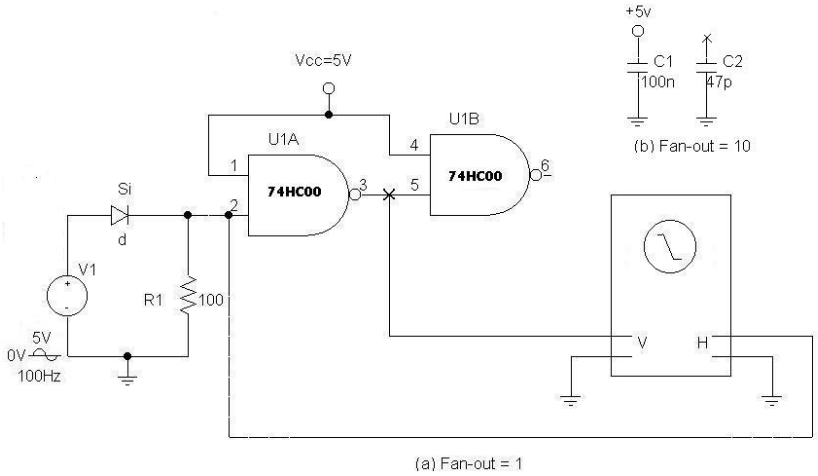


Figure 4.1

3. Carefully sketch the VTC of the circuit, labeling all asymptotic voltages and breakpoints. Do this for:
(a) A fan-out 1, as in Figure 3.1(a)
(b) A fan-out of 10, as in Figure 3.1(b) Connect 100nF bypass capacitor as close to device as possible.

4. In order to determine relationship between power dissipation and frequency, connect the circuit as shown in Figure 4.2 and apply 5 V square wave to the input of the gate and connect miliammeter series between V_{DD} and V_{DD} pin of device. Connect 100nF bypass capacitor as close to device as possible.

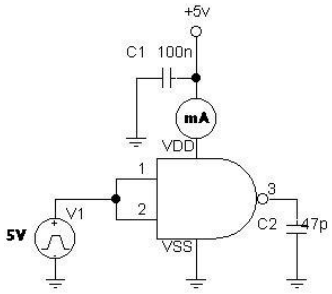


Figure 4.2

5. Measure and record current drawn from the gate for frequencies given below.

Frequency	100 Hz	1kHz	10kHz	100kHz	1MHz
Supply current					

Table 4.1

6. Examine table of power dissipation. What happens to the power dissipation as the frequency goes up? Give the reasons.
7. Remove the 50 pF load (fan-out of 10) capacitance and note the effect on the supply current with a 1MHz input signal on the gate. Explain effect of load on V_{DD}.
8. Connect 50 pF load capacitance to the output again and connect an oscilloscope probe to the supply line next to IC and select ac coupling on oscilloscope.
9. Apply 1 MHz square-wave to input of gate and observe the V_{DD} voltage trace.
10. While continuing to monitor V_{DD} with oscilloscope, remove 100nF bypass capacitor and observe the waveform procuded on V_{DD} by the 1MHz input to the gate. Measure and record this unwanted voltage on V_{DD}. Explain the unwanted voltage.