

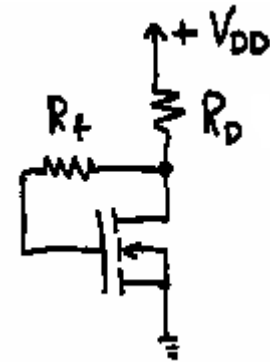
1. The n-channel MOSFET in the circuit has the following parameters:

$$K = 1 \text{ mA/V}^2,$$

$$V_{GS(Th)} = 2 \text{ V}.$$

$$V_{DD} = 10 \text{ V and } R_f = 1 \text{ M}\Omega.$$

- Draw the MOSFET characteristics and the load lines for $R_D = 100\Omega$ and $1\text{K}\Omega$ on the same graph of $I_D - V_{GS}$.
- For these cases, calculate the exact I_D and V_{GS} values.

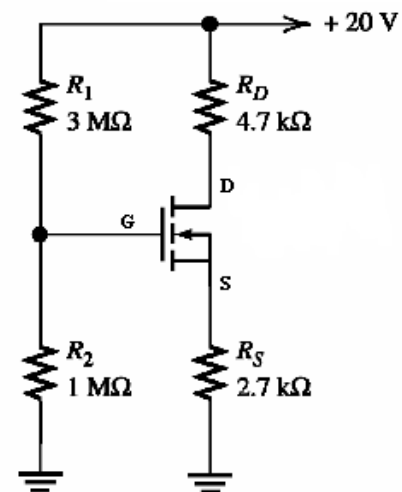


2. The n-channel MOSFET in the circuit has the following parameters:

$$K = 1 \text{ mA/V}^2,$$

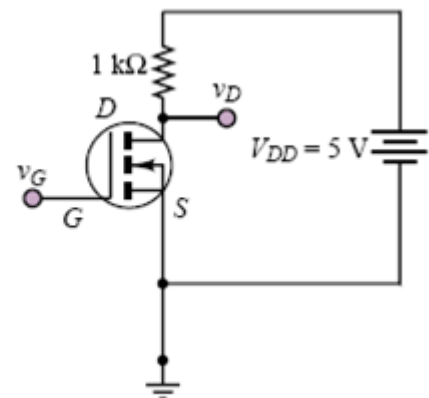
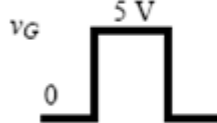
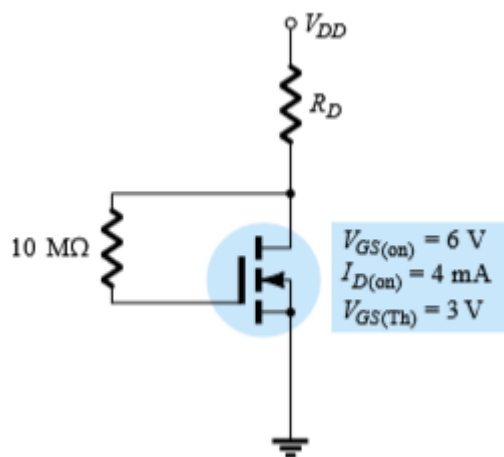
$$V_{GS(Th)} = 2 \text{ V}.$$

Find I_D and V_{DS} .



3) Example 6.17 p.287, Boylestad 7th

The levels of V_{DS} and I_D are specified as $V_{DS} = \frac{1}{2}V_{DD}$ and $I_D = I_{D(on)}$ for the network of Fig. 6.53. Determine the level of V_{DD} and R_D .

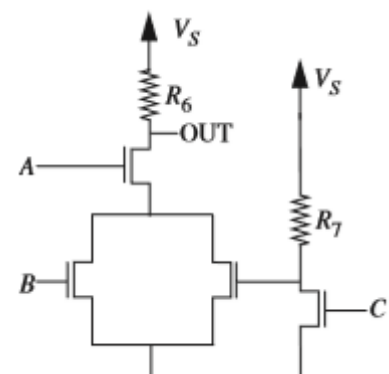


4) The NMOS transistor shown in the figure has $V_T = 1.5 \text{ V}$, $k = 0.4 \text{ mA/V}^2$. If v_G is a pulse with 0 V to 5 V, find the voltage levels of the pulse signal at the drain output.

(That is; find v_D for $v_G = 0$ and for $v_G = 5 \text{ V}$)

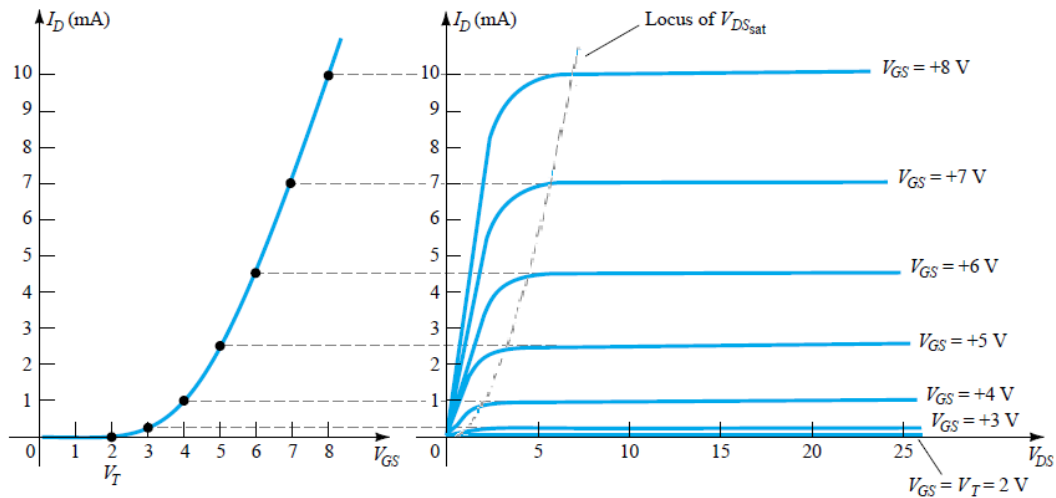
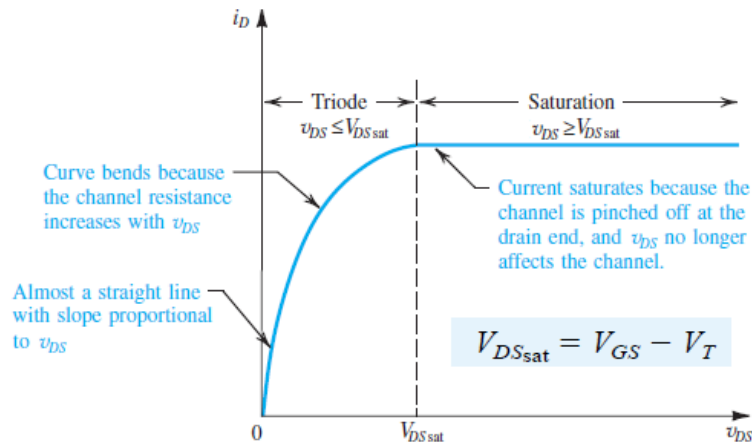
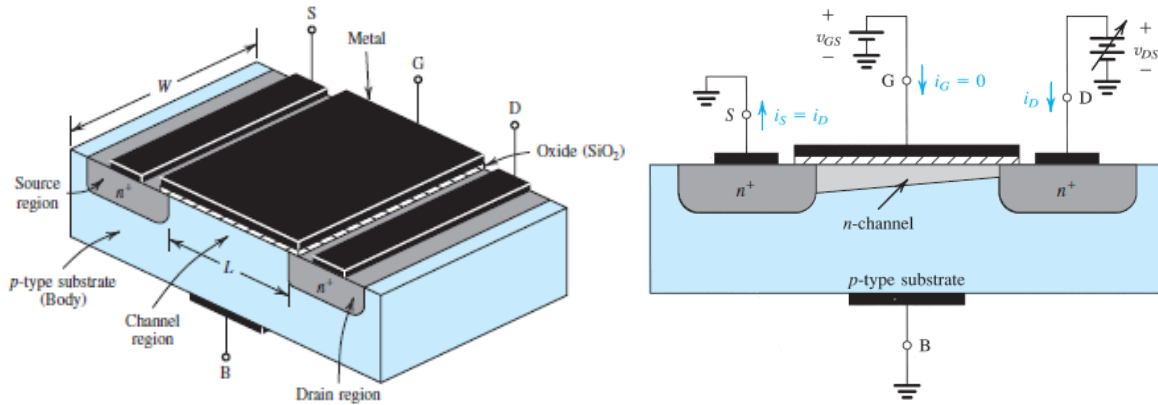
5) Using the MOSFET in Question 4, and resistors, design two input NOR and NAND gates.

6) What is the logic function implemented by the circuit given.



7) How can we make a (1-bit) memory cell using MOSFETs?

Enhancement-Type MOSFETs

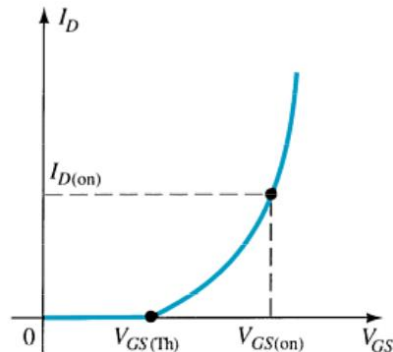


$I_G = 0\text{ A}, I_D = I_S$

V_T
 $I_{D(on)}$
 $V_{GS(on)}$

$I_D = k (V_{GS} - V_{GS(Th)})^2$

$k = \frac{I_{D(on)}}{(V_{GS(on)} - V_{GS(Th)})^2}$



- If $V_{GS} < V_{GS(Th)}$, the NMOS is in cut-off, $I_D = 0$. Otherwise:
- If $V_{DS} < V_{GS} - V_{GS(Th)}$, the NMOS is in Triode (Ohmic) region, in this case:

$$I_D = k[2(V_{GS} - V_{GS(Th)})V_{DS} - V_{DS}^2]$$
- If $V_{DS} \geq V_{GS} - V_{GS(Th)}$, the NMOS is in Saturation region, in this case:

$$I_D = k(V_{GS} - V_{GS(Th)})^2$$