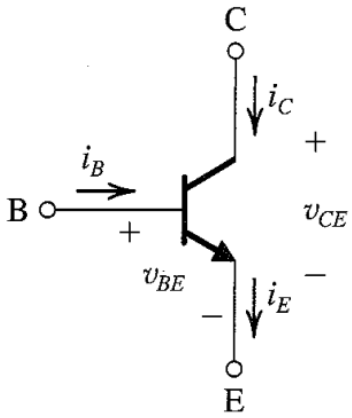
Here, an npn transistor is considered, for a pnp transistor all the voltage and current directions need to be reverted.



Note that, due to KCL, we always have: $i_E = i_B + i_C$

Transistor is a nonlinear device, and, mainly it has three modes of operation:

Active Mode (operation in the linear region):

Here the transistor behaves as a current controlled current source.

$i_C = \beta i_B$ $v_{BE}=0.7$

This mode is valid only if $i_B > 0$ and $v_{CE} > v_{CE(sat)}$

Cut-Off Mode (not enough voltage is provided for BE junction):

Here the transistor behaves as open circuit.

$i_B = 0$ $i_C = 0$

This mode is valid only if $v_{BE} < 0.7$

Saturation Mode (too much current is pumped into the base terminal):

Here the transistor voltages become constant. v_{CE} is almost zero. i_C is stuck on the limit.

$v_{BE}=0.7$ $v_{CE} = v_{CE(sat)}$

This mode is valid only if $i_B > 0$ and $i_C < \beta i_B$

Hints for DC Analysis:

1. Assume the active mode first. Use the two equations provided. Since you know the voltage v_{BE}, try writing KVL loop equations involving the v_{BE} voltages. Avoid using v_{CE} in the equations because we do not know this voltage at this stage.

2. Solve the equations and obtain the currents. Calculate v_{CE} voltages.

3. If validity conditions are satisfied, we are done. Otherwise:

   a. If the resulting i_B is less than zero, the transistor is at cut-off. Analyze the circuit using the cut-off mode model.

   b. If the resulting v_{CE} is less than $v_{CE(sat)}$, the transistor is at saturation. Analyze the circuit using the saturation mode model.

5. If validity conditions are satisfied in this case we are done. If not, all combinations of modes of operations may need to be checked for all transistors in the circuit.

6. Still not valid? There is something wrong in the circuit design.